Reg. No. ☐☐☐☐☐☐☐☐☐☐☐☐☐

## Question Paper Code : 21155

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2014.

Seventh Semester

Electrical and Electronics Engineering

CS 1358 — COMPUTER ARCHITECTURE

(Common to Electronics and Instrumentation Engineering/
Instrumentations and Control Engineering and
Sixth Semester Electronics and Communication Engineering)

(Regulation 2008)

Time : Three hours                                                    Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What are the main functional units of computer?

2. What are the main advantages of addressing modes?

3. Define overflow.

4. Write the IEEE notation for floating point.

5. Define cycle.

6. List out the different methods of generating control signal by the processor.

7. Draw the SRAM cell diagram.

8. What is the need to include the cache memory?

9. Why I/O device and processor should be synchronized?

10. Define Exceptions.

PART B — (5 × 16 = 80 marks)

11. (a) (i) With a neat block diagram explain the basic operational concepts. (8)

    (ii) Explain what is Big–Endian and Little–Endian. (8)

Or

    (b) (i) What are the different bus structures available? Describe it. (8)

    (ii) Describe the different addressing modes with example. (8)

12. (a) (i) With diagram explain the carry look ahead adder. (8)

    (ii) With circuit explain the binary division algorithm. (8)

Or

    (b) (i) Explain the Combinatorial array multiplier. (8)

    (ii) Describe how the CSA speeds up the addition. (8)

13. (a) (i) Brief about the control sequence execution of a instruction ADD. (8)

    (ii) What are the advantages of pipelining? Explain with example the instruction level pipelining. (8)

Or

    (b) (i) What are the methods available for grouping the control signals? Write the advantages and disadvantages of those methods. (8)

    (ii) Define data Hazard. Describe how the execution speed of a processor can be increased. (8)

14. (a) (i) What is meant by fast page mode? Describe the operations of Synchronous DRAM. (8)

    (ii) How the virtual memory increase the size of the memory system? Explain the address translation by Associative–mapped TLB. (8)

Or

    (b) (i) What is meant by cache coherent problem? Describe the Set associative mapping method. (8)

    (ii) How the data are stored in RAID1? Explain it. (8)

15. (a) What is the disadvantage of program-controlled I/O accessing method? What is the solution for that? Explain it.

Or

    (b) How is DMA used to access the I/O? Describe it.

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2

21155